CLAIMS

Please amend the claims as follows:

1. (amended) A system for initializing a data processing system, comprising:

a plurality of parameter registers;

a ~~user-defined~~ hardware initialization ~~input~~ port capable of receiving ~~defining~~ a first set of user-definable initialization data utilized for initializing said data processing system;

a serial non-volatile memory, coupled to said plurality of parameter registers, said serial non-volatile memory utilized for storing a second set of initialization data utilized for initializing said data processing system;

a parallel non-volatile memory, coupled to said plurality of parameter registers, said parallel non-volatile memory utilized for storing a third set of initialization data utilized for initializing said data processing system; and

a multiplexor interposed between said parameter registers and said ~~user-defined~~ hardware initialization ~~input~~ port, said serial non-volatile memory, and said parallel non-volatile memory, wherein said multiplexer determines ~~for determining~~ a selected set of initialization data ~~selection~~ from among said first, second and third sets of initialization data ~~user-defined initialization input, said serial non-volatile memory, and said parallel non-volatile memory~~ and relays ~~relaying~~ said selected set of initialization data ~~selection~~ to said plurality of parameter registers, in response to a control signal, such that said data processing system is initialized from an uninitialized state to a minimal level of operation utilizing said selected set of initialization data.

2. (amended) The system for initializing a data processing system according to claim 1, further including a set of control resistors coupled to a user-defined control input signal, wherein said set of control resistors outputs said control signal in response to said user-defined control input signal.

3. (amended) The system for initializing a data processing system according to claim 1, further including a set of initialization resistors coupled to ~~a~~ the ~~user-defined~~ hardware initialization ~~input~~ port to provide said first set of user-definable initialization data, wherein said set of

initialization resistors outputs said first set of user-definable initialization data to said hardware initialization port ~~an initialization signal,~~ in response to an ~~said user defined~~ initialization input signal.

4. (amended) The system for initializing a data processing system according to claim 1, further including:

a processor; and

a command decoder ~~is~~ interposed between said multiplexor and said processor and said parallel non-volatile memory, wherein said command decoder filters ~~is utilized for filtering~~ commands issued from said processor for a set of desired commands.

5. (amended) The system for initializing a data processing system according to claim 1, further including a serial non-volatile memory controller ~~is~~ interposed between said serial non-volatile memory and said multiplexor, wherein said serial non-volatile memory controller controls ~~is utilized for controlling~~ data output by said ~~sent from~~ serial non-volatile memory.

6. (amended) The system for initializing a data processing system according to claim [[1]] 4, further including a parallel non-volatile memory controller ~~is~~ interposed between said parallel non-volatile memory and said command decoder, wherein said parallel non-volatile memory controller controls data output by said ~~is utilized for controlling data sent from~~ parallel non-volatile memory.

7. (amended) A data processing system, comprising:

a processor;

a memory, coupled to said processor; and

a system for initializing the ~~a~~ data processing system, including ~~comprising~~:

a plurality of parameter registers;

a ~~user defined~~ hardware initialization port capable of receiving ~~input~~ ~~defining~~ a first set of user-definable initialization data utilized for initializing said data processing system;

a serial non-volatile memory, coupled to said plurality of parameter registers, said serial non-volatile memory utilized for storing a second set of initialization data utilized for initializing said data processing system;

a parallel non-volatile memory, coupled to said plurality of parameter registers, said parallel non-volatile memory utilized for storing a third set of initialization data utilized for initializing said data processing system; and

a multiplexor interposed between said parameter registers and said ~~user-defined~~ hardware initialization port ~~input~~, said serial non-volatile memory, and said parallel non-volatile memory, wherein said multiplexor selects a selected set of initialization data from among said first, second and third sets of initialization data ~~for determining a selection from said user-defined initialization input, said serial non-volatile memory, and said parallel non-volatile memory~~ and ~~relaying~~ relays said ~~selection~~ selected set of initialization data to said plurality of parameter registers, in response to a control signal;

wherein said data processing system initializes from an uninitialized state to a minimal level of operation utilizing said selected set of initialization data.

8. (original) A host data processing system, comprising:

an integrated circuit in which a data processing system in accordance with claim 7 is fabricated;

an interconnect coupled to said integrated circuit;

a host processor; and

a host memory.

9. (amended) A method of initializing a data processing system, said method comprising:

sending a control signal to a multiplexor, said control signal designating one of a plurality of sets of initialization data as a preferred set of initialization data for initializing said data processing system, said plurality of sets of initialization data including:

a first set of user-definable initialization data accessible at a hardware initialization port of the data processing system;

a second set of initialization data accessible in a serial non-volatile memory; and

a third set of initialization data accessible in a parallel non-volatile memory;

in response to the control signal, the multiplexor relaying said preferred set of initialization data to a plurality of parameter registers; and

utilizing said preferred set of initialization data stored in said plurality of parameter registers to initialize said data processing system from an uninitialized state to a minimal level of operation.

10. (original) The method of initializing a data processing system according to claim 9, ~~further including:~~ wherein sending a control signal to a multiplexor comprises sending said control signal in response to receipt of ~~generating~~ a signal~~, by a user, from~~ at a ~~user-defined~~ hardware control input port ~~to send said control signal to said multiplexor~~.

11. (original) The method of initializing a data processing system according to claim 9, further including:

a command decoder filtering commands ~~by a command decoder, said commands~~ issued from a processor, in response to designating said third a set of initialization data ~~stored in a parallel non-volatile memory~~ as said preferred set of initialization data.

12.-14. (canceled)